**RISC-V Class Project Phase 10 – Cache Optimization**

Phase 10 of the Class Project optimizes a cache design based on Codasip simulation of a configurable cache. This exemplifies another very common function in Computer Architecture, which is to optimize the design of a system component based on a set of parameters. As always, the selection of an appropriate Benchmark program or programs which closely approximate the expected application is critically important.

You will receive a unique Benchmark, which is a test program, and a standard Codasip CA model including a cache. The exercise will be to modify the cache parameters of the design and simulate the Benchmark using it. The Benchmark includes a cost calculator which will display the cost of the Benchmark running on the specific design, and the goal is to find the cache design which minimizes the cost.

A significant component of Phase 10 is the creation of a report which explains the process used to find the optimal design.

1. **Copy the Hardware Project**

Import the Phase10\_orig project from G:/Information/Phase 10. Rename the project to standardname10 and build it with Simulator (ca). Note that the cache component has significantly increased the complexity of the Codasip code, so building the simulator will take several minutes. The cache is in a new file model/ca/pipelines/ca\_pipe\_stageca\_me.codal. You may be interested in looking at this file but knowledge of it is not necessary for Phase 10.

1. **Copy the Benchmark Test**

Import the standardname10\_test project from your H: folder, which will be available once you have successfully completed Phase 8. Phase 9 is not required to begin Phase 10. Change the SDK to one of your valid Assemblers – standardname5/6/7/8. Build the Benchmark. You will see several warnings during the build which are OK.

1. **Determine the Baseline Cost**

Run the Benchmark on your baseline design, which has the cache disabled. Note that running the benchmark may take a couple of minutes. Upon completion, the test will report information on the hit ratio of the run. The cost of the run will be in register x30. Note this cost, as other designs will be compared to it.

1. **Optimize the Cache by Modifying the Parameters**

The optimization process consists of updating some of the cache parameters, running the benchmark on the updated design and noting the cost. The objective of the exercise is to determine the cache design (i.e. the parameters) which minimizes the cost function. As parameters are changed, note how the cost changes. This will provide information on how the cache design affects the cost which will be a good guide to determining further changes to reduce the cost. The process is described below.

* 1. **Modify the Parameters**

The cache parameters are defined in lines 266 through 269 of the ca\_defines.hcodal file, which are shown in Figure 1.

**Text

Description automatically generated**

Figure 1

There are 4 parameters which can be modified. Do NOT modify anything else in the hardware project.

CACHEMODE – this parameter specifies if there is a cache (CACHEMODE = 0 if no cache) and if there is a cache whether it is a Writethrough Cache (CACHEMODE = 1) or a Writeback Cache (CACHEMODE = 2).

CWDS – this parameter specifies the number of 32-bit words in a Cache Line, in a value which is the log2 of the actual value. Valid values are 0 (1 word per Cache Line), 1 (2 words per Cache Line) and 2 (4 words per Cache Line).

MWDS – this parameter specifies the number of 32-bit words in a Memory Line, in a value which is the log2 of the actual value. Valid values are 0 (1 word per Cache Line), 1 (2 words per Cache Line) and 2 (4 words per Cache Line). This is the number of words transferred between the Cache and memory in each operation, and transferring a Cache Line may require multiple memory transfers. MWDS must be less than or equal to CWDS.

CAC\_INDEX – this parameter specifies the number of Cache Lines in the Cache, in a value which is the log2 of the actual value. Examples are 3 (8 lines in the cache), 5 (32 lines in the cache) and so on. The minimum value for this parameter is 2 and the maximum is 7.

The initial values in Phase10\_orig set CACHEMODE to 0 (no cache), in which case none of the other parameters are used and can be any value.

* 1. **Exercise the New Hardware Design**

Once a new set of parameters have been entered, build the hardware design and run your Benchmark on it. This will produce the cost for this hardware configuration in register x30.

* 1. **Iterate to Find the Minimum Cost**

Continue modifying the hardware design and testing it until you believe you have identified the optimal configuration (i.e. the one with the minimum cost). Keep track of each iteration as you run it – the values of each of the 4 parameters and the cost associated with that combination. A good place to do this is in the Table of the report you will create below.

* 1. **Useful Information in the Test Results**

Several other registers contain useful information at the end of the run, which can help guide the selection of configurations.

x3 – the total number of cycles executed. Note that this is not the same as the cycles reported in the Debug Window, as there are some calculations made in the Benchmark to reduce simulation time.

x4 – the total number of memory operations (loads and stores)

x5 – the total number of accesses to Main Memory

x22 – the cost associated with the cycles executed

x23 – the cost associated with the selected Cache Mode

x24 – the cost associated with the width of the Memory Line

x25 – the cost associated with the size of the Cache (Cache Line size x # of Cache Lines)

1. **Create the Project Report**

Once the optimal configuration has been identified, the next step is to complete the Project Report. Download the Phase 10 Report template file from the Phase 10 area of Canvas. Rename the report template to standardname10.docx. Each section of the Report must be completed.

* 1. **Describe the Optimization Process**

The results of each attempt should be described in the order they were made – what parameters were selected, why they were selected and the resulting cost. The included Table should be filled in with results in the order they were tested, and it is a good idea to add additional information (as described in Section 4.4 above) which helped guide the process. Describe how the results of each attempt influence the selection of the next attempt as the optimization proceeds. A minimum of 10 attempts must be described.

* 1. **Define the Final Configuration**

Once the final parameters are identified, the Final Configuration section of the report must be completed. This includes the following information:

INPUT PARAMETERS – the parameters which were selected

SIZE – how many data bytes are contained in the cache (not counting any tag bits)

FIELDS – specify the widths of the four fields which comprise the processor address

TRANSFER CYCLES – how many memory cycles are required for a cache line transfer

1. **Scoring**

Phase 10 is worth 2.5% of the overall score with a potential bonus of 1.75%, so the maximum score will be 175 points if the full bonus is achieved. The time-based bonus of 1% will be awarded for each day the project is submitted before the Target Date, and a 4% deduction is taken for each day after the Target Date.

The normal score is a function of how close the final solution is to the optimal configuration. If the optimal cost is achieved, 100 points will be awarded. 95 points will be awarded for identifying the second lowest cost, and so on down to 5 points for the 20th best configuration. There are approximately 750 different possible configurations, so a thoughtful approach is required to minimize the number of attempts you make, but there is no limit to the number of attempts.

The bonus score is determined by the Project Report. 2 points are awarded for each attempt reported with the correct cost value, up to 10 attempts. 5 points will be awarded for each correct parameter as specified in Section 5.2 other than the INPUT PARAMETERS (there are 6 parameters). Up to 25 points will be awarded based on the quality of the optimization process and the description of it.

1. **Exporting the Project**

The final configuration of the standardname10 project should be submitted to G:/Submission in the normal way, and the Project Report should be included in the Slack DM sent to the Professor.

1. **Important Note**

This is the first semester that we have used this particular version of Phase 10, so there are more likely to be typos and confusing descriptions in this document than you normally see. Please report these as soon as you see them in #phase10, and I will probably issue additional versions of this document as these are discovered.